2023 ACADEMIA SINICA
EARLY-CAREER INVESTIGATOR
RESEARCH ACHIEVEMENT AWARD

方 劭 云

國立臺灣科技大學電機工程學系教授

代表著作：

- T.-C. Yu, **S.-Y. Fang**, H.-S. Chiu, K.-S. Hu, P. H.-Y. Tai, C.-F. C Shen, and H. Sheng, "Pin Accessibility Prediction and Optimization with Deep Learning-Based Pin Pattern Recognition," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 40, no. 11, pp. 2345-2356, November 2021.
- G.-Q. Fang, Y. Zhong, Y.-H. Cheng, and **S.-Y. Fang**, "Obstacle-Avoiding Open-Net Connector with Precise Shortest Distance Estimation," *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, vol. 39, no. 5, pp. 1096-1108, May 2020.
- Y.-J. Jiang and **S.-Y. Fang**, "COALA: Concurrently Assigning Wire Segments to Layers for 2D Global Routing," accepted in May 2022, *IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems (TCAD)*.

簡評：

方教授利用機器學習模型，以創新的方法預測可能違反規則的電路設計，此一技術已成功整合到商業工具中，並被國際電子電路設計公司廣泛使用。

簡歷：

方劭云於 2013 年取得國立臺灣大學電子工程學研究所博士，並於同年進入國立臺灣科技大學電機工程系任教。方劭云的研究領域為電子設計自動化，研究重點其一為針對半導體先進製程技術提出各式實體設計最佳化演算法，其二為利用機器學習開發實體設計與製造可行性設計最佳化技術；研究成果廣受各界肯定，為吳大猷先生紀念獎與國內多項年輕學者研究獎項之獲獎人。

方劭云與其研究團隊除了發表多篇電子設計自動化領域國際頂尖期刊與會議論文，亦多次獲得國際積體電路電腦輔助設計軟體製作競賽前三名，並與新思科技股份有限公司和台灣積體電路製造股份有限公司進行多年期產學合作，實質幫助業界於先進製程的技術開發。

Shao-Yun Fang received her Ph.D. from the Graduate Institute of Electronics Engineering at National Taiwan University in 2013. In the same year, she joined the Department of Electrical Engineering at National Taiwan University of Science and Technology as a faculty member. Shao-Yun Fang's research primarily focuses on electronic design automation (EDA). One of her key research areas involves developing various physical design optimization algorithms for advanced semiconductor manufacturing processes. Another area involves utilizing machine learning to develop optimization techniques for physical design and design for manufacturability. Her research achievements have been widely recognized and has received the Wu Ta-You Memorial Award and multiple national young scholar research awards.

Shao-Yun Fang and her research team have not only published numerous papers in top international journals and conferences in the field of EDA but have also consistently achieved top-three rankings in the CAD Contest at ICCAD, the largest international academic research competition in EDA. Additionally, they have established long-term partnerships with companies like Synopsys and Taiwan Semiconductor Manufacturing Company (TSMC), contributing significantly to the industry's advancement in cutting-edge technologies.

代表作簡介：

隨著製程節點的不斷縮小，標準元件變得更小且數量大幅增加，標準元件的接腳可觸性成為低可繞度的主要問題之一，並導致可觀的設計規則違反。為了應對這個問題，許多先進的研究利用基於機器學習技術進行設計規則違反的預測，這些模型使用全域繞線擁塞度和接腳密度作為主要特徵訓練模型，但先進製程中的設計規則違反並不一定與此二特徵強烈相關。在此代表作中，我們提出了文獻上第一個以接腳圖案作為主要特徵的機器學習預測模型，直接識別給定的接腳圖案是否會因低可觸性而造成設計規則違反，此模型亦可以應用於引導實體設計階段的細部擺置過程以直接最佳化整體接腳可觸性。

With the continuous scaling down of process nodes, standard cells become much smaller and cell counts are dramatically increased. Pin accessibility becomes one of the major issues causing design rule violations (DRVs). To tackle this problem, many recent works apply machine-learning-based techniques to predict whether a local region has DRV or not by regarding global routing congestion and local pin density as the main features during the training process. Empirically, however, DRV occurrence is not necessary to be strongly correlated with the two features in advanced nodes. In this representative publication, we propose the first work of deep-learning-based DRV prediction using pin pattern as our major feature to directly identify whether a DRV will exist or not due to bad pin accessibility of the given pin pattern. In addition, unlike most of the existing models that can only be used for DRV prediction, the proposed models can be applied to guide detailed placement for pin accessibility optimization during physical design.

得獎感言：

首先感謝中央研究院年輕學者研究成果獎評審委員的肯定、指導教授臺大張耀文老師的栽培鼓勵、和臺科大電機系同仁與前輩們對我的照顧。也感謝我們研究團隊的學生們的努力和善良可愛，讓我能持續對教學與研究工作抱有高度熱忱。最後要感謝我的父母、先生、兒子、與朋友，你們支持、陪伴、與豐富我的人生，讓我能在工作生活平衡後，獲得更好的工作表現。

Firstly, I would like to express my gratitude for the recognition from the Young Scholar Research Award committee at Academia Sinica, the supervision and encouragement from my advisor, Prof. Yao-Wen Chang at National Taiwan University, and the support provided by my colleagues and seniors in the Department of Electrical Engineering at National Taiwan University of Science and Technology. I would also like to extend my appreciation to the hardworking and kind-hearted students in our research team, whose dedication has kept my passion for teaching and research. Lastly, I want to thank my parents, husband, sons, and friends for their unwavering support, companionship, and enrichment of my life.